# M.Sc. 4th Semester Examination, 2012

## ELECTRONICS

*(Advanced Electronics Lab)*

(Practical)

PAPER—ELC-405

*Full Marks* : 50

*Time* : 3 hours

**Answer any one question from either *PSPICE* or *Digital Electronics***

*The questions are of equal value*

*Candidates are required to give their answers in their own words as far as practicable*

*Illustrate the answers wherever necessary*

## *PSPICE*

In each of the following questions, you have to save the design file by "your roll no., -design" and then save the plot in a file "your roll no.-plot".

*Marks Distribution ( For PSPICE )*

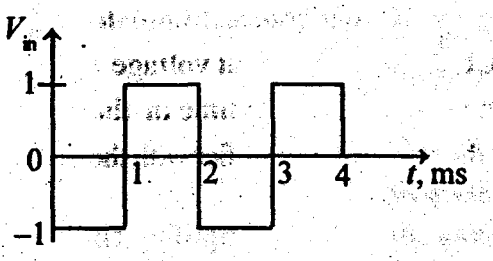
| | |
|---|---|
| Theory | – 07 |
| Circuit Design | – 10 |
| Simulation | – 10 |
| Verification and Accuracy | – 05 |
| Discussion | – 03 |
| Viva | – 10 |
| Laboratory Note Book | – 05 |

1. Design an inverting amplifier circuit using op-amp taking input resistor $R_1 = 470\ \Omega$, feedback resistor $R_2 = 4{\cdot}7\ k\Omega$ and load resistor $R_3 = 10\ k\Omega$. Apply sine wave as an input signal with suitable amplitude and frequency of your choice. Simulate the circuit using PSPICE and plot the input voltage $V_{in}$ versus time and output voltage $V_0$ versus time in the same graph. Also verify the gain of the amplifier with the given value.

2. Design a non-inverter amplifier circuit using op-amp taking input resistor $R_1 = 1\ k\Omega$, feedback resistor $R_2 = 10\ k\Omega$ and load resistor $R_3 = 10\ k\Omega$. Apply sine wave as an input signal with suitable amplitude and frequency of your choice. Simulate the circuit using

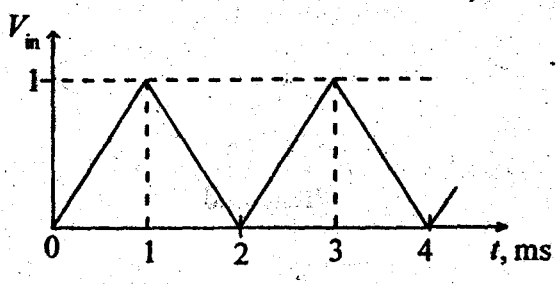
PSPICE and plot the input voltage $V_{in}$ versus time and output voltage $V_0$ versus time in the same graph. Also verify the gain of the amplifier with given value.

3. Design an integrator circuit using op-amp taking input resistor $R_1 = 1\ k\Omega$, feedback resistor $R_2 = 6{\cdot}8\ k\Omega$, feedback capacitor $C_2 = 0{\cdot}1\ \mu F$ and load resistor $R_3 = 10\ k\Omega$. Simulate the circuit using PSPICE and plot the transient response of the output voltage for a duration of 0 to 4 ms in steps of 50 μs for the input voltage given below.




4. Design a differentiator circuit using op-amp taking input resistor $R_1 = 1\ k\Omega$, input capacitor $C_1 = 0{\cdot}4\ \mu F$, feedback resistor $R_2 = 6{\cdot}8\ k\Omega$ and load resistor $R_3 = 10\ k\Omega$. Simulate the circuit using PSPICE and

plot the transient response of the output voltage fo
duration of 0 to 4 ms in steps of 10 μs for the inp
voltage given below.




5. Design a first order low pass active filter with cut-o
frequency 3 kHz in PSPICE. Simulate the circuit and pl
the gain versus frequency curve. Also verify the cut-o
frequency of the plot with its given value.

6. Design a first order high pass active filter with cut-o
frequency 1 kHz in PSPICE. Simulate the circuit and pl
the gain versus frequency curve. Also verify the cut-o
frequency of the plot with its given value.

7. Design a second order active low pass Butterwor
filter with cut-off frequency 3 kHz. Simulate the circu
using PSPICE and plot the gain versus frequency curv
Also verify the cut-off frequency with the given valu

8. Design a second order active high pass Butterworth filter with cut-off frequency 1 kHz. Simulate the circuit using PSPICE and plot the gain versus frequency curve. Also verify the cut-off frequency with the given value.

9. Design an astable multivibrator circuit with frequency 1 kHz and duty cycle 66.67% using IC 555. Simulate the circuit using PSPICE and plot the output versus time curve. Also verify the output frequency and duty cycle with the given values.

( *Digital Electronics* )

*Marks Distribution* ( *For Digital* )

| | |
|---|---|
| Theory | — 05 |
| Circuit Design | — 15 |
| Implementation | — 07 |
| Experimental Result | — 05 |
| Discussion | — 03 |
| Viva | — 10 |
| Laboratory Note Book | — 05 |

10. Design a 4-bit synchronous odd counter using JK flip-flop. Verify the count sequence by LED display.

11. Design a 4-bit synchronous even counter using JK flip-flop. Verify the count sequence by LED display.

12. Design a 4-bit ripple counter using JK flip-flop. Verify the count sequence by LED display.

13. Design a mod 6 synchronous up counter using JK flip-flop. Verify the count sequence by LED display.

14. Design a mod 6 synchronous down counter using JK flip-flop. Verify the count sequence by LED display.