M.Sc. 2nd Semester Examination, 2012

ELECTRONICS

(*Digital Electronics*)

PAPER—ELC-202

(Theory)

Full Marks : 50

Time : 2 hours

Answer **Q. No. 1** and any **three** from the rest

The figures in the right-hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

1. (*a*) Why R-2R ladder type DAC is preferred over a weighted resistor type DAC ? Explain.

(*b*) What is burning of EPROM ? How EPROM is erased ?

(*c*) How many clock are required to convert an analog signal to the digital form using SAR type ADC ?

(*d*) Give an example of self dual function and prove self duality.

(*e*) Draw the schematic diagram of a practical sample-hold circuit using MOSFET. 2 × 5

2. (*a*) If $f = \overline{B}\overline{C} + (A \oplus B)C$ and $g = A \oplus B \oplus C$ then using Karnaugh map show that $f \oplus g = \overline{A} + C$.

(*b*) Let $F = B\overline{C}D + \overline{A}BC\overline{D}$ and $F_1 = \overline{B} + \overline{C}\overline{D} + \overline{A}C\overline{D}$. Find F_2 such that $F = F_1 \cdot \overline{F}_2$. Find the simplest solution of F_2. 5 + 5

3. (*a*) What is multiplexer tree ?

(*b*) Implement the following multi-output combitional logic circuit using 4 to 16-line decoder.

$F_1 = \Sigma m(1, 2, 4, 7, 8, 12, 13)$
$F_2 = \Sigma m(2, 3, 9, 11)$
$F_3 = \Sigma m(10, 12, 13, 14)$
$F_4 = \Sigma m(2, 4, 8)$

(c) Show the schematic diagram, to obtain 16 × 8 memory using 16 × 4 memory ICs. 10

4. Show that the following circuit adds two single binary bits 'a' and 'b' with the carry input C_{in}. Is it possible to avoid using the two inverters at the output of z_1 and z_2 if $\overline{a}$, $\overline{b}$ and $\overline{c_{in}}$ are used as inputs. 5 + 5

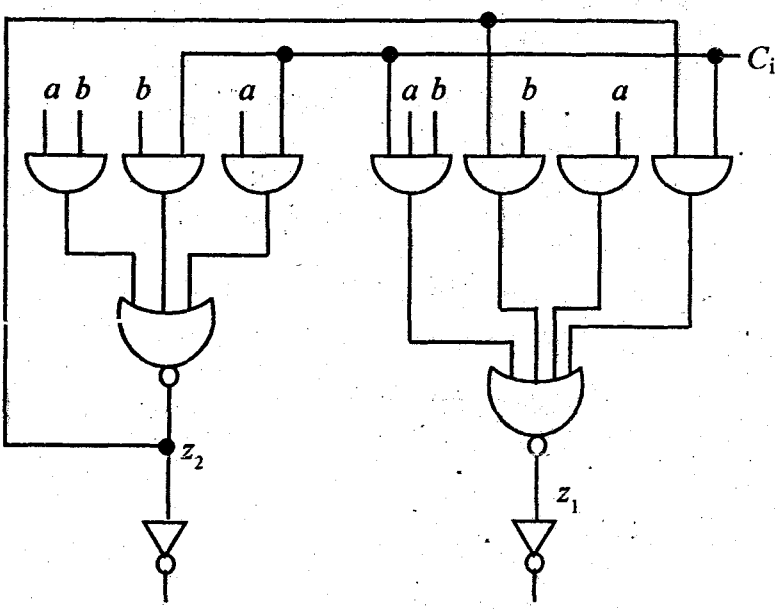

Fig. 1

5. (*a*) What is charged couple device ? What are the advantages of it over shift register ? State its working principle with suitable diagram.

   (*b*) Explain with a diagram, the working principle of MOSFET, NOR gate. (1 + 2 + 3) + 4

6. Three partners : Mr. Ajoy, Mr. Bimal and Mr. Chetan decided to select the president of their organization through voting secretly using voting machine among them.

   (*a*) Develop a appropriate truth table.

   (*b*) From the results of (*a*), design a logic circuit that provides an output of logic-1, whenever the majority vote is 'Yes'. Be sure to finish a mnimum implementation.

   (*c*) Modify the logic diagram of voting machine of part (*b*) so that all 'NOR' gates are used. 4 + 3 + 3

[*Internal Assessment* : 10 Marks]