2024

M.Sc. 2nd Semester Examination

MCA

PAPER : MCA–201

(Advanced Computer Architecture)

Full Marks : 100

Time : 3 hours

The figures in the right-hand margin indicate marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer from **both** the Groups as directed.

GROUP—A

Answer *any* **five** questions : 2×5=10

1. What is super scalar design?

2. What do you mean by MMU?

3. State any three properties of RISC.

4. What is SIMD computer architecture?

5. Define structural hazard.

6. Explain stack based organization.

7. Distinguish between Harvard and Von Neumann architecture.

8. What is ISA?

GROUP—B

Answer *any* **four** questions : 15×4=60

9. *(a)* With a diagram, explain synchronous model of linear pipelining.

(b) How can you determine clock period of a *K*-stage linear synchronous pipeline? If a 3-stage linear synchronous pipeline unit has stage delay 3ns, 2ns and 5ns, respectively and latch delay 1ns. Determine the clock period.

(c) Distinguish between linear and non-linear pipeline units.

(d) Explain instruction pipeline. 4+5+3+3

10. *(a)* consider a *K*-stage pipeline unit with clock period *t*. For execution of *n* task, derive the expression to calculate speed up, efficiency and throughput.

(b) Obtain the initial collision vector.

(c) Draw state transition diagram.

(d) List all simple and greedy cycles.

(e) Calculate minimal average latency.

4+2+5+2+2

16. Write short notes on *any* **three** of the following : 5×3=15

(a) Micro-programmed control unit

(b) Set-associative mapping technique of cache memory

(c) Data hazard

(d) Interrupt-initiated I/O mode of data transfer

[Internal Assessment : 30]

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(b) Determine the maximum throughput of the same pipeline unit.

(c) Discuss VLIW processor with diagram. 6+4+5

11. *(a)* What is addressing mode? What is its advantage?

(b) Explain register direct, register indirect and relative addressing modes.

(c) Compare among logical, circular and arithmetic shift operations.

(d) Discuss the steps of communication between application program and I/O interface with proper diagram. 3+6+3+3

12. *(a)* What is Flynn's classification of computer? Draw and explain SIMD architecture.

(b) Discuss COMA model of multiprocessor with a proper diagram.

(c) Explain the difference between UMA and NUMA models of multiprocessor. 6+5+4

13. *(a)* Explain the following terms :

Cost, Size, Access time, Unit of transfer and Bandwidth of hierarchical memory organization.

(b) What is locality of reference property of memory hierarchy? Explain different types of locality of references.

(c) Define access frequency and effective access time. 6+5+4

14. *(a)* What is virtual memory? What are the advantages and disadvantages of it?

(b) A three-level memory system having cache access time of 15 ns and disk access time of 80 ns has a cache hit ratio of 0·96 and main memory hit ratio of 0·9. What should be the main memory access time to achieve effective access time of 25 ns?

(c) Explain segmentation technique with diagram. 4+5+6

15. Consider the following reservation table of a non-linear pipeline processor for function *P*

		— Clock —							
		1	2	3	4	5	6	7	8
Stages	S_1	P					P		P
	S_2		P		P				
	S_3			P		P		P	

(a) Find out all forbidden and non-forbidden latencies.