PG/IIS/MCA/201/25

MCA 2nd Semester Examination, 2025

MCA

(*Advanced Computer Architecture*)

PAPER — MCA-201

Full Marks : 100

Time : 3 hours

Answer all questions

The figures in the right hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable
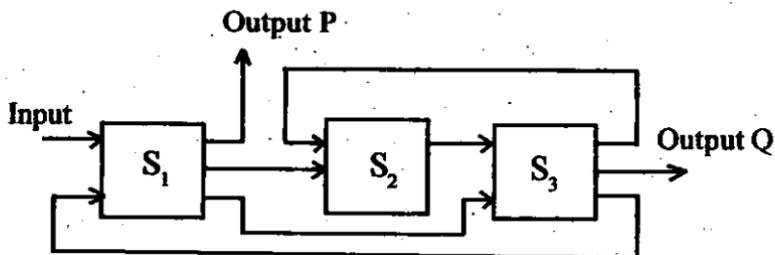
GROUP—A

Answer any **five** questions :   2 × 5

1. What is structural hazard ? How can you reduce structural hazard ?

2. Perform arithmetic left shift and logical left shift operations of 11101010.

3. What is the difference between NUMA and COMA model of multi-processor?

4. What is systolic array?

5. Distinguish between super pipeline design and super scalar design.

6. Consider a 5-stage linear synchronous pipe-line unit with stage delays 5ns, 4ns, 9ns, 7ns, and 3ns and latch delay of 1ns. Determine the clock frequency of the pipeline unit.

7. Define MFLOPS.

8. List all types of connections of the following non-linear pipeline unit :

Output P

Input

S_1 S_2 S_3

Output Q

GROUP – B

Answer any **four** questions : 15×4

9. (a) What are I/O driver and I/O interface ? Give a diagram to show the steps of communication between application program and I/O interface.

   (b) In a simple machine with load-store architecture having clock rate 50 MHz, let the instruction frequency be as follows for a program :

Operations	Frequency	No. of clock cycles
ALU	40	1
Load	20	2
Store	10	2
Branch	30	2

Calculate MIPS.

(c) Computers M_1 and M_2 are two imple-mentations of the same instruction set. M_1 has clock rate of 50 MHz and M_2 has clock rate of 75 MHz. M_1 has a CPI of 2.8 and M_2 has a CPI of 3.2 for a given program. How many times M_2 is faster than M_1 ?   6 + 4 + 5

10. (a) What is data hazards ?

(b) Explain different type of data hazards.

(c) Consider three consecutive instructions I_1, I_2 and I_3 as follows :

I_1 : ADD R_1, R_2 // $R_1 \leftarrow R_1 + R_2$

I_2 : ADD R_3, R_4 // $R_3 \leftarrow R_3 + R_4$

I_3 : SUB R_1, R_3 // $R_1 \leftarrow R_1 + R_3$

(i) Find out domain of instruction of all above three instructions.

(ii) Find out range of instruction of all above three instructions.

(iii) Check the necessary condition of WAR, RAW, and WAW hazards to know hazard may occur or not.

$$1 + 6 + (2 + 2 + 4)$$

11. Consider the following reservation table of a non-linear pipeline processor for function Q :

— Clock→

		1	2	3	4	5	6
	S_1	Q				Q	
Stages	S_2			Q			
	S_3		Q		Q		Q

(a) Find out all forbidden and non-forbidden latencies.

(b) Obtain the initial collision vector

(c) Draw state transition diagram.

(d) List all simple and greedy cycles.

(e) Calculate minimal average latency.

$$4 + 2 + 5 + 2$$

12. (a) Distinguish between RISC and CISC.

(b) Compare the number of instructions and clock cycles needed to evaluate $Z = X^* Y + W$ using :

(i) A CISC instruction MULADD Z, X, Y, W (1 instruction, 1 cycle)

(ii) RISC instructions using separate multiply and add (each taking 1 cycle)

(c) Define execution time. A processor executes the following instructions with given cycles :

Load : 2 cycles	Given
Add : 1 cycle	LOAD R1, A
Store : 2 cycles	LOAD R2, B
	ADD R3, R1, R2
	STORE R3, C

Calculate the total execution time in cycles.   4 + 6 + 5

13. (a) Explain the terms : Speed up, efficiency, and throughput.

(b) Determine the maximum Speed up of a k-stage pipeline unit.

(c) Consider a 5-state linear pipeline processor with a clock rate of 40 MHz. Calculate speed up, efficiency and throughput for 20000 instructions.

$$6 + 4 + (2 + 2 + 1)$$

14. (a) Draw and explain MIMD architecture.

(b) What is UMA model of multiprocessor ? Discuss with a proper diagram.

(c) For a multi-computer system with startup time (latency)= 10 microseconds, length of the message = 8,192 bytes, and bandwidth of the link = 10 MB/s, calculate the total message passing time in microseconds. $5 + 5 + 5$

15. (a) What is inclusion property of memory hierarchy ? Explain two polices to maintain coherence property of memory hierarchy.

(b) Compare among temporal, special, and sequential locality of reference.

(c) A three-level memory system having cache access time of 15ns, main memory access time of 27 ns and disk access time of 80ns has a cache hit ratio of 0.96 and main memory hit ratio of 0.9. What should be the effective access time ? Also calculate efficiency of the memory system.   6 + 3 + 6

16. (a) What is instruction format ? Given an ISA with 16-bit instructions, design a simple instruction format to support 256 opcodes, and 16 registers. Encode the instruction ADD R3, R5 where ADD is the first opcode of the list of opcode.

(b) Two ISAs, A and B, have the following characteristics :

ISA A has 3-address instructions
(e.g., ADD R1, R2, R3)
ISA B has 2-address instructions
(e.g., ADD R1, R2)

Write a sequence of instructions for both ISAs to compute $X = (A + B) - (C + D)$. Count the total number of instructions used in each ISA.

(c) What is addressing mode ? For each of the following instructions, identify the addressing mode : 4 + 6 + 5

(i) MOV R1, # 45

(ii) MOV R2, (R3)

(iii) MOV R4, 1000(R2)

(iv) MOV R5, [1234]

[Internal Assessment — 30 Marks]

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